INFORMATION DISCLOSURE CITATION FORM FOR PATENT APPLICATION (FORM PTO-1449) (Substitute)	Docket No.: YOR920030139US1 Serial No.: Applicant(s): Chirag S. PATEL Filing Date: Group:

U.S. PATENTS

Initials	Patent Number	Issue Date	Name	Class	Sub-class	Filing date

FOREIGN PATENT DOCUMENTS

Initials	Document Number	Date	Country	Name	Translation? Yes/No/n/a

OTHER DOCUMENTS (Title, Author, Date, Pages, Etc., if known)

	S. Kiyono et al, Consideration of Chip Circuit Damages on DCS-FBGA Packages
	Wu, L., Wang, Y. P., Hsiao C. S., "Innovative Stack-Die Package – S2BGA
	M. Sunohara et al., Development of Wafer Thinning and Double-Sided Bumping
	Technologies for the Three-dimensional Stacked LSI, all three presented at
	52nd Electronic Components and Technology Conference, May 2002, San Diego, CA
	Intel Stacked Chip Scale Packaging Products, available at
	http://www.intel.com/design/flcomp/prodbref/298051.htm

Examiner's Signature:	Date Considered:

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